REMARKS/ARGUMENTS

1. Claim objections

Claims 1 and 15 have been amended to more clearly define "identical device characteristic" as "identical structure". This is supported throughout the specification (at least Paragraphs [0032] and [0050] as published) and drawings (at least Fig.4 and Fig.11) as the definition of a basic unit and no new material has been introduced. Additionally, claim 15 has be amended from "a plurality of basic unit" to "a plurality of basic units" as required. Reconsideration of claims 1 and 15 over these objections is respectfully requested.

2. Claim rejections

Claims 1 and 15 are rejected under obviousness-type double patenting over claim 1 of Wang et al (US 6,902,957). Claims 1 and 15 are rejected under obviousness-type double patenting over claim 1 of Wang (US 6,902,957) in view of Friend et al. (US 2003/0140080). Claims 1-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang et al. Claims 1-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Friend et al. Claims 1-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Gheewala et al. (US 6,445,065).

Without disclaimer of any kind, claims 4, 9-11, and 19-22 have been cancelled.

The present application discloses the use of a plurality of identical basic units, which can be programmed via a metal layer to form a wide variety of clocked or non-clocked circuits without regard to the location of the respective circuits on the semiconductor substrate.

With this in mind, claims 1 and 15 have been amended to include the limitations that a clocked circuit is formed by forming traces to program one or more basic units and that a non-clocked circuit is formed by forming traces to program a different set of

one or more basic units (paragraph [0031], [0032] as published).

Concerning Wang et al, the present invention further teaches a clocked logic circuit comprising at least two of the basic units of which at least one of the at least two basic units is programmed to be isolated from a clock feed.

Because of at least these differences, reconsideration of all rejections involving Wang et al, is respectfully requested.

Concerning Friend et al., Friend may disclose that a domino logic gate can be used as clocked logic circuit by using different signals on the transistor gates 211 and 219 or used as non-clocked logic circuit by the two transistors 211 and 219 being off in [0062] and [0063] and the associated Fig. 3. Please note that Friend discloses a domino logic gate used as clocked logic circuit or non-clocked logic circuit by the signaling of the two transistors rather than the layout layer. However, each of the basic unit of Friend needs to be connected to clock. By utilizing the layout layer in the present invention, the basic unit is not limited to be connected to clock and the claims carry the limitation that it is the layout layer that respectively forms the clocked or the non-clocked circuit. Friend does not meet this limitation.

Because of at least these differences, reconsideration of all rejections involving Friend et al, is respectfully requested.

Concerning Gheewala et al., the abstract states "all asynchronous core cells are placed in a first region and all synchronous core cells are placed in a second region'' which is clearly different than the claimed limitation of "without placing restrictions on positions of the clocked logic circuit and the non-clocked logic circuit on the semiconductor body".

In the rejection of claims 1 and 15, the Examiner references col. 20-24 of Gheewala to show teachings of the above cited claim limitation. Although unable to find cols. 20-24, in Col.5, lines 20-24 the applicant located statements similar to those cited by the Examiner. It is noted that although the text may state "high-drive cells are placed throughout the integrated circuit without any restrictions", the applicant is unable to

locate any text specifically teaching allowing placement of non-clocked circuit without restriction, as is claimed in both claims 1 and 15.

Perhaps at least as relevant is Col. 6, lines 29-55 which clearly teaches that the core cells (basic units) of asynchronous cells 220 are different than the core cells of synchronous cells 240, are of different sizes (Col.5, lines 54-64), and are said by Gheewala to be distinct (Title, Abstract, Col.6, lines 39-42, Fig.4, Fig.7A-B).

Gheewala teaches separate clocked and non-clocked regions and utilizes different structured "basic units" in each of these regions and thus does not appear to anticipate the present claims. Because of at least these differences, reconsideration of all rejections involving Gheewala et al, is respectfully requested.

3. New claims

The applicant wishes to introduce new claims 23-28 for consideration. All new claims are supported at least by Fig.9 and no new material has been introduced. The applicant is unable to locate any teachings in known prior art alone or in combination of the specific method claimed in new independent claim 23 or the specific device of new independent claim 26 or of the respective dependent claims 24-25 and 27-28.

Sincerely yours,

Winston Hsu Date: 09.29.2006

Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

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